



Information Disclosure Statement

USPN 10/824,569

October 12, 2004

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Form PTO-1449 (Modified) Page 1 of 3	ATTY DOCKET NO. B-5327NP 621691-8	U.S. SERIAL NO. 10/824,569
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS Todd KAPLAN	
	FILING DATE April 13, 2004	GROUP not yet assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB- CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
la	5,684,482	11/1997	Galton	341	144	
	5,982,317	11/1999	Steensgaard-Madsen	341	143	
	6,137,431	10/2000	Lee et al.	341	161	
	6,211,805 B1	4/2001	Yu	341	155	
	6,271,782 B1	8/2001	Steensgaard-Madsen	341	143	
	6,326,912 B1	12/2001	Fujimori	341	143	
	6,348,884 B1	2/2001	Steensgaard-Madsen	341	118	
	6,373,424 B1	4/2002	Soenen	341	161	
	6,437,718 B1	8/2002	Oyama et al.	341	143	
	6,441,759 B1	8/2002	Raghavan et al.	341	143	
	6,456,218 B1	9/2002	Dedic et al.	341	144	
	6,469,646 B1	10/2002	Song	341	144	
	6,473,011 B1	10/2002	Steensgaard-Madsen	341	118	
	6,496,129 B2	12/2002	Dedic et al.	341	144	
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	6,531,973 B2	3/2003	Brooks et al.	341	143	
	6,556,158 B2	4/2003	Steensgaard-Madsen	341	131	
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	6,633,248 B2	10/2003	Song	341	144	
la	6,661,362 B2	12/2003	Brooks	341	143	

EXAMINER <i>Paul H. Geyer</i>	DATE CONSIDERED <i>12/29/04</i>
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FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

L	Galton, I., "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> , Vol. 44, No. 10, pp. 808-817 (October 1997).
↑	Geerts, Y., et al., "A 2.5M Sample/s Multi-Bit $\Delta\Sigma$ CMOS ADC with 95dB SNR," <i>IEEE International Solid-State Circuits Conference Digest of Technical Papers</i> , pp. 336-337, 468 (2000).
↑	Hernandez, L., et al., "Programmable Sine Wave Generator Employing a Mismatch-Shaping DAC," <i>ICECS Dig. Tech. Papers</i> , pp. 135-138 (1998).
↑	Jensen, H.T., et al., "A Reduced-Complexity Mismatch-Shaping DAC for Delta-Sigma Data Converters," <i>IEEE</i> , pp. I-504-I-507 (1998).
↑	Kaplan, T., et al., "A 1.3-GHz IF Digitizer Using A 4th-Order Continuous-Time Bandpass $\Delta\Sigma$ Modulator," <i>IEEE 2003 Custom Integrated Circuits Conference</i> , Session 7-5, pp. 127-130 (2003).
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↑	Lin, H., et al., "A Bandpass Mismatch-Shaped Multi-Bit $\Sigma\Delta$ Switched-Capacitor DAC Using Butterfly Shuffler," <i>1999 IEEE International Solid-State Circuits Conference Digest of Technical Papers</i> , pp. 58-59 (1999).
↑	Miller, M.R., et al., "A Multibit Sigma-Delta ADC for Multimode Receivers," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 38, No. 3, pp. 475-482 (March 2003).
↑	Park, Yong-In, et al., "A 16-Bit, 5MHz Multi-Bit Sigma-Delta ADC Using Adaptively Randomized DWA," <i>IEEE 2003 Custom Integrated Circuits Conference</i> , pp. 115-118 (2003).
↑	Razavi, B., <i>Design of Analog CMOS Integrated Circuits</i> , McGraw-Hill, pp. 309-310 (2001).
L	Sakina, Y., "Multi-Bit $\Sigma\Delta$ Analog-To-Digital Converters with Nonlinearity Correction Using Dynamic Barrel Shifting," <i>Electronics Research Laboratory, College of Engineering, University of California, Berkeley, Memorandum No. UCB/ERL M93/63</i> , pp. 1-73 (July 26, 1993).

EXAMINER <i>Paul Van Guler</i>	DATE CONSIDERED <i>12/24/04</i>
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	FILING DATE April 13, 2004	GROUP not yet assigned

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h	Welz, J., et al., "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> , Vol. 48, No. 11, pp. 1014-1027 (November 2001).

EXAMINER <i>hulten</i>	DATE CONSIDERED <i>12/29/04</i>
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